Trials@uspto.gov
Tel: 571-272-7822

Paper 7
Entered: August 8, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TOSHIBA CORPORATION, TOSHIBA AMERICA, INC.,
TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.,
and TOSHIBA AMERICA INFORMATION SYSTEMS, INC.,
Petitioner,

v.

INTELLECTUAL VENTURES II LLC,
Patent Owner.

Case IPR2014-00418
Patent 5,500,819

Before KEVIN F. TURNER, TREVOR M. JEFFERSON,
and DAVID C. McKONE, *Administrative Patent Judges.*

JEFFERSON, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., and Toshiba America Information Systems, Inc. (collectively "Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1–11 and 17–19 of U.S. Patent No. 5,500,819 (Ex. 1001, "the '819 patent"). *See* 35 U.S.C. § 311. Intellectual Ventures II LLC ("Patent Owner") filed a Preliminary Response (Paper 6, "Prelim. Resp.").

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides as follows:

> THRESHOLD.—The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Upon consideration of the Petition and the Preliminary Response, we conclude that Petitioner has established a reasonable likelihood that it would prevail with respect to claims 1–11 and 17–19 of the '819 patent. Accordingly, we institute an *inter partes* review of claims 1–11 and 17–19 of the '819 patent.

B. Related Matters

Patent Owner has sued Petitioner for infringement of the '819 patent in *Intellectual Ventures I LLC v. Toshiba Corporation, Toshiba America, Inc.*, No. 1:13-cv-00453 (D. Del.). Pet. 1; Paper 5 (Patent Owner's Mandatory Notices).

C. References Relied Upon

Petitioner relies upon the following prior art references:

Ex. 1003, Ogawa, US 4,745,577, issued May 17, 1988, filed Nov. 15, 1985 ("Ogawa '577");

Ex. 1005, Ogawa, US 4,773,045, issued Sept. 20, 1988, filed Oct. 16, 1985 ("Ogawa '045"); and

Ex. 1006, Ogawa, Japanese Patent Application H3-46832, published Jul. 17, 1991 (Japan priority application 59-245802 for Ogawa '577) ("JP '832").

D. The Asserted Grounds

Petitioner contends that the challenged claims are unpatentable based on the following grounds (Pet. 7-8):

Reference(s)	Basis	Claims challenged
Ogawa '577	§ 102(b)	1–6 and 17–19
Ogawa '577, Ogawa '045 and JP '832	§ 103(a)	1–6 and 17–19
JP '832	§ 102(b)	7–11
JP '832, Ogawa '577, and Ogawa '045	§ 103(a)	7–11

E. The '819 Patent

The '819 patent, titled "Circuits, Systems and Methods for Improving Page Accesses and Block Transfers In A Memory System," issued on Mar. 19, 1996, and addresses control circuitry that controls the exchange of data between read/write circuitry and first and second slave circuitry. Ex. 1001, Abstract. The '819 patent discloses circuits for improving page accesses and block transfers in memory. *Id*. at 1:7–10. The "invention provide[s] for the construction of a memory which includes an array of volatile memory cells, address decode circuitry

for selecting rows and/or columns of cells in the memory array, and master sense amplifier circuitry for reading and writing data into those selected cells." *Id*. at 2:52–57. The invention also includes "[a]t least two sets of latching circuitry . . . coupled to the master sense amplifiers for temporarily storing data being exchanged with the master sense amplifiers during read and write operations to the array of memory cells." *Id*. at 2:57–61.

Figure 2 of the '819 patent, shown below, provides an exemplary block diagram of the memory system disclosed.

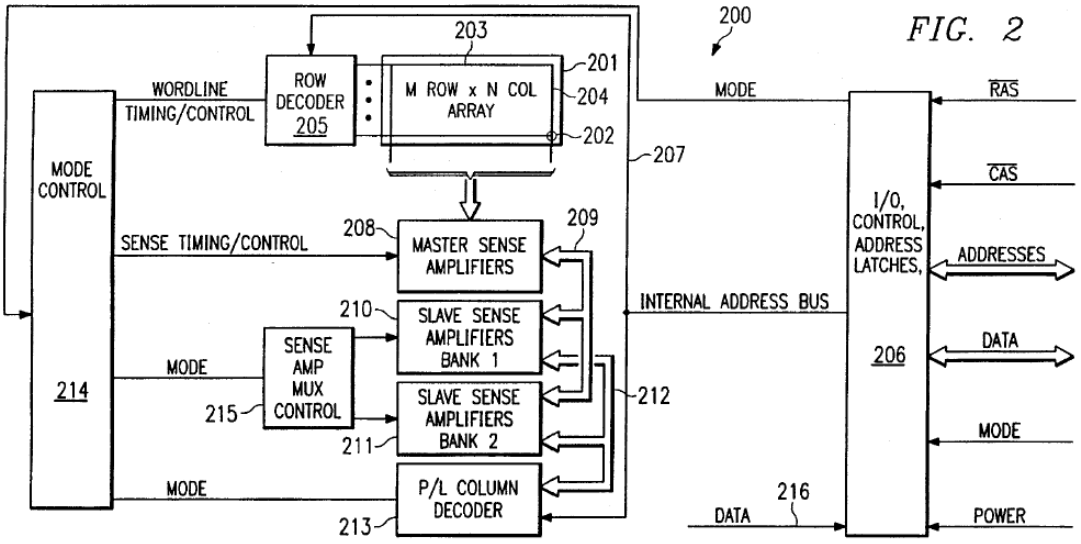


Figure 2 depicts a block diagram of memory system 200 with an M x N array of flash memory cells 201, with wordlines (rows) 203 and bitlines (columns) 204. *Id*. at 5:52–57; 3:25–26. Representative memory cell 202 is located at the intersection of wordline 203 and bitline 204. *Id*. at 5:58–60. "[Bitlines] 204 of memory array 201 are coupled to a bank 208 of master sense amplifiers[,]" which are coupled via "bus 209 to a first bank 210 (bank 1) of slave sense amplifiers and a second bank 211 (bank 2) of slave sense amplifiers." *Id*. at 6:8–12. "Slave sense amplifier banks 210 and 211 are further coupled by a local data I/O bus 212 to

column decoder circuitry 213." *Id*. at 6:12-14. The challenged claims are directed to a memory that includes control circuitry that controls the sensing of data from cells via the master sense amplifiers, the temporary storage of those data in the first and second bank of slave sense amplifiers, and the rewriting of those data back in the memory array at the same or different locations.

F. Illustrative Claims

Illustrative independent claims 1, 7, and 17 are reproduced below:

> 1. A memory comprising:
>
> an array of rows and columns of volatile memory cells;
>
> addressing circuitry for providing access to selected ones of said memory cells;
>
> master read/write circuitry for reading and writing data into said selected ones of said cells;
>
> first slave circuitry for storing data for exchange with said master read/write circuitry;
>
> second slave circuitry for storing data for exchange with said master read/write circuitry; and
>
> control circuitry for controlling exchange of data between said master read/write circuitry and said first and second slave circuitry, said control circuitry operable during a move operation to:
>
> control sensing by said master read/write circuitry of data from a said row in said array selected by said addressing circuitry;
>
> control transfer of said data from said master read/write circuitry to a selected one of said first and second slave circuitry; and
>
> control writing of said data through said master read/write circuitry to a second said row in said array selected by said addressing circuitry.

7. A memory system comprising:

an array of memory cells arranged in rows and columns, each said row associated with a conductive wordline and each said column associated with a conductive bitline;

a row decoder coupled to said wordlines;

a bank of master sense amplifiers coupled to said bitlines;

a plurality of banks of slave sense amplifiers coupled to said master sense amplifiers;

a column decoder coupled to each of the plurality of banks of slave sense amplifiers; and

control circuitry coupled to said row decoder, said bank of master sense amplifiers and said banks of slave sense amplifiers, said control circuitry including mode control circuitry coupled to said row decoder and said master sense amplifiers and multiplexer control circuitry coupled to said mode control circuitry and said plurality of banks of slave sense amplifiers, said control circuitry operable during a move operation to:

control sensing by said master sense amplifiers of data from a said row in said array selected by said row decoder;

control transfer of said data from said master sense amplifiers to a selected one of said banks of slave sense amplifiers;

control writing of said data through said master sense amplifiers to a second said row in said array selected said row decoder.

17. A method of performing a block transfer within a memory including an array of memory cells arranged in rows and columns, each said row

> associated with a conductive wordline and each said column associated with a conductive bitline, comprising the steps of:
>
> selecting a row in the array;
>
> sensing the bitlines of the array to read data stored in the cells of the selected row with a bank of master sense amplifiers;
>
> latching the data read from the cells of the selected row in a bank of slave sense amplifiers;
>
> writing the data stored in the slave sense amplifiers through the master sense amplifiers to different cells in the array.

II. ANALYSIS

A. Claim Construction

We determine the meaning of the claims as the first step of our analysis. The Board interprets claims using the broadest reasonable construction. *See* 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Claim terms generally are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998).

Petitioner asserts that claim terms should be given their ordinary and customary meanings, as the patentee did not act as a lexicographer or provide special meaning for any claim terms. Pet. 8. Patent Owner has not disputed

Petitioner's conclusion and provides no alternate construction for any claim terms on this record.

Accordingly, based on the present record, we determine that no express claim construction is necessary for any claim term for purposes of this decision.

B. Asserted Grounds of Unpatentability

1. Anticipation of Claims 1–6 and 17–11 by Ogawa '577 (Ex. 1003)

Petitioner contends that Ogawa '577 (Ex. 1003) anticipates claims 1–6 and 17–19. Pet. 9–12, 13–16 (claim charts). Petitioner relies on the Declaration of Robert J. Murphy (Ex. 1004) ("Murphy declaration") and provides claim charts showing the claim limitations and the corresponding disclosure in Ogawa '577 (Pet. 13–19; 30–37). Petitioner's analysis of the challenged claims also cites Ogawa '045 and JP '832 to support the anticipation contentions. Pet. 10–12; 13–37. Petitioner contends that citations to these earlier references (Ogawa '045 and JP '832) by the same inventor of Ogawa '577 show the inventor's knowledge at the time of Ogawa '577 with respect to memory write operations. Pet. 10–12.

a. Ogawa '577 (Ex. 1003)

Ogawa '577 describes "[a] semiconductor memory device with shift registers used for a video RAM." Ex. 1003, Abstract. Ogawa '577 discloses "a memory cell array, bit lines, and word lines, a pair of shift registers, and transfer gate circuits arranged between the bit lines and the shift registers." *Id.* Figure 2 of Ogawa '577, reproduced below, shows a semiconductor memory device with shift registers. *Id.* at 2:10–12.

Fig. 2

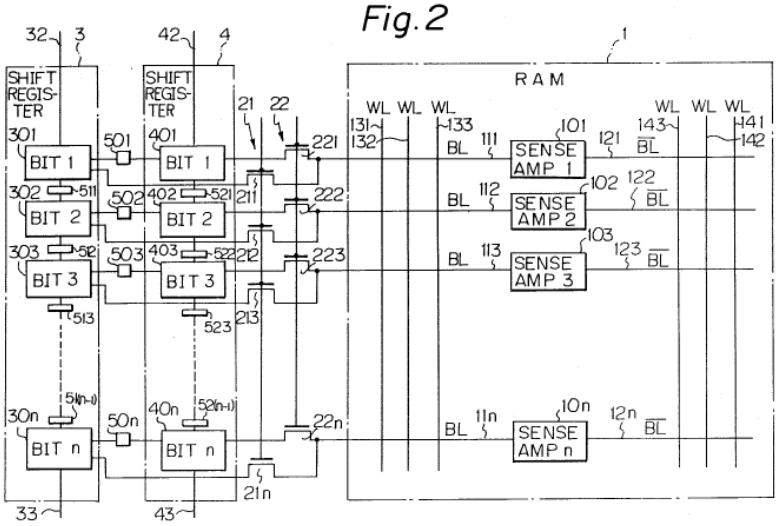


Figure 2 of Ogawa '577 shows "a dynamic RAM 1 of an open bit-line type, groups of transfer gates 21 and 22, and shift registers 3 and 4." *Id*. at 3:19–21. Data are provided via input lines 32 and 42 of shift registers 3 and 4. Data also are delivered through output lines 33 and 43 from shift registers 3 and 4. *Id*. at 3:22–25. Figure 2 shows that RAM 1 includes sense amplifiers 101, 102, . . . 10n; bit lines (BL) 111, 112, . . . 11n; word lines (WL) 131, 132, . . . 13n; and bit lines ($\overline{BL}$) 121, 122 . . . 12n. *Id*. at 3:29–36. Ogawa '577 discloses that shift registers 3 and 4 can be used for reading and writing in various combinations for the parallel transfer of data between registers and for a scroll display operation.

b. Analysis

In support of Petitioner's contentions that Ogawa '577 anticipates claims 1–6 and 17–19, Petitioner relies heavily on the knowledge of one of ordinary skill in the art and the doctrine of inherency. *See e.g.*, Pet. 16 (stating that Ogawa '577 inherently discloses control circuitry); 17 (stating that "one of ordinary skill in the art would have recognized that the control circuitry" controls sensing by the sense amplifiers of Ogawa '577). Indeed, Patent Owner contends that Petitioner relies

on inherency 13 times in its analysis of independent claims 1 and 17. Prelim. Resp. 2–3. Patent Owner further contends that Petitioner fails to show that the teachings identified in Ogawa '577 as inherent are necessarily present and not merely common or expected in the art. Prelim. Resp. 3.

We agree with Patent Owner that Petitioner has not demonstrated that specific claim limitations are taught expressly or inherently. Under 35 U.S.C. § 102, a prior art reference anticipates a patent claim if it expressly or inherently describes each and every limitation set forth in the claim. *See Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987). Inherent anticipation applies when the missing claim element is inherent, or necessarily present, in the recited reference. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999).

Claims 1 ("control writing of said data through said master read/write circuitry to a second said row in said array selected by said addressing circuitry") and 17 ("writing the data stored in the slave sense amplifiers through the master sense amplifiers to different cells in the array") recite that control circuitry writes data through the master read/write circuitry or master sense amplifiers to a second row of the array. Petitioner identifies sense amplifiers (101, 102, . . . 10n of Figure 2 in Ogawa '577) as the master read/write circuitry of claim 1 and master sense amplifiers of claim 17. Pet 16; 30–31.

Petitioner's contentions for independent claims 1 and 17 rely on the knowledge of one of ordinary skill in the art to show that Ogawa '577 discloses writing data through the sense amplifiers into the memory cells on the BL and $\overline{\text{BL}}$ sides (right side and left side) of Figure 2 in Ogawa '577. Pet. 20–24 (discussing claim limitation [1i]); 30–32 (discussing claim limitation [17d]). Specifically,

Petitioner argues that the scroll display operation in Ogawa '577 (Ex. 1003, 4:6–18) discloses reading data from BL (right side) of the memory through the sense amplifiers (101, 102, . . . 10n) in Figure 2, through shift registers 3 and 4, and writing those data to $\overline{BL}$ (left side) of the memory through the sense amplifiers. Pet. 17–20 (claim limitation [1i]); 30–32 (claim [17d] limitation relying on claim [1i]).

We are not persuaded by Petitioner's reasoning that the scroll operation discloses expressly that shift register 4 writes data through sense amplifiers to the left side or $\overline{BL}$ of Figure 2. Pet. 18. The scroll display operation only states that shift register 4 is used for writing but fails to state where the data are written. Ex. 1003, 4:6–18 (stating the "shift register 3 is used for reading, while the shift register 4 is used for writing" and that "data of the shift register 4 is supplied to the immediately preceding word line for which scanning has already been completed"). We are unpersuaded by Petitioner's argument that Ogawa '577 describes expressly how data are written to $\overline{BL}$ (left side).

We also are not persuaded by Petitioner's contentions that Ogawa '577 discloses, inherently, writing to the $\overline{BL}$ (left side) of the memory shown in Figure 2. Pet. 17–24; 30–32. Petitioner's arguments rely on "common practice" knowledge of one of ordinary skill in the art based on the open bit line architecture of Figure 2 in Ogawa '577. Pet. 20 (stating that it was "common to use . . . sense amplifiers"). Common practice, however, does not disclose that the sense amplifiers of Figure 2 in Ogawa '577 necessarily write to both the left and right sides of Figure 2 as required to show inherently the writing of data recited in claims 1 and 17. *See In re Montgomery*, 677 F.3d 1375, 1379-80 (Fed. Cir. 2012) ("A reference may anticipate inherently if a claim limitation that is not expressly

disclosed 'is necessarily present, or inherent, in the single anticipating reference.'" (quoting *Verizon Servs. Corp. v. Cox Fibernet Va., Inc*., 602 F.3d 1325, 1336 (Fed. Cir. 2010)).

Petitioner's citations to the Murphy declaration (Ex. 1004) also do not support that one of ordinary skill in the art would have understood that Ogawa necessarily discloses using the same sense amplifiers to drive the bitlines BL and $\overline{BL}$ on the left and right sides of Figure 4. Pet. 19–24 (citing Ex. 1004 ¶¶ 27–32). Petitioner's argument and the Murphy declaration testimony, that it would have been a "natural design approach" to use sense amplifiers to drive all the bitlines BL and $\overline{BL}$ connected to the cells in the memory array in Figure 2 rather than add additional circuitry for writing data (Pet. 23), belie the assertion that Ogawa '577 *necessarily* discloses using sense amplifiers to drive the bitlines BL and $\overline{BL}$ on the left and right sides of Figure 2. *See* Pet. 20 ("common approach to achieve [claimed feature] in an open bit-line architecture"); 23 ("natural design approach"); Ex. 1004 ¶ 31 ("natural design approach"). Indeed, Petitioner's argument acknowledges that additional circuitry could have been used to write data to the memory array. Pet. 23; *see* Prelim. Resp. 12–13.

Petitioner's arguments and evidence do not support a reasonable likelihood that Ogawa '577 expressly or inherently discloses the limitations of claim 1 (limitation [1i]) or claim 17 (limitation [17d]). Petitioner's arguments for independent claims 1 and 17, and dependent claims 2–6 and 18, 19, rely on the same inherency arguments presented for claim 1, limitation [1i]. *See* Pet 20–24; 30–32. Based on the foregoing, Petitioner has not shown a reasonable likelihood that it will prevail as to independent claims 1 and 17, and dependent claims 2–6 and 18, 19, as anticipated by Ogawa '577.

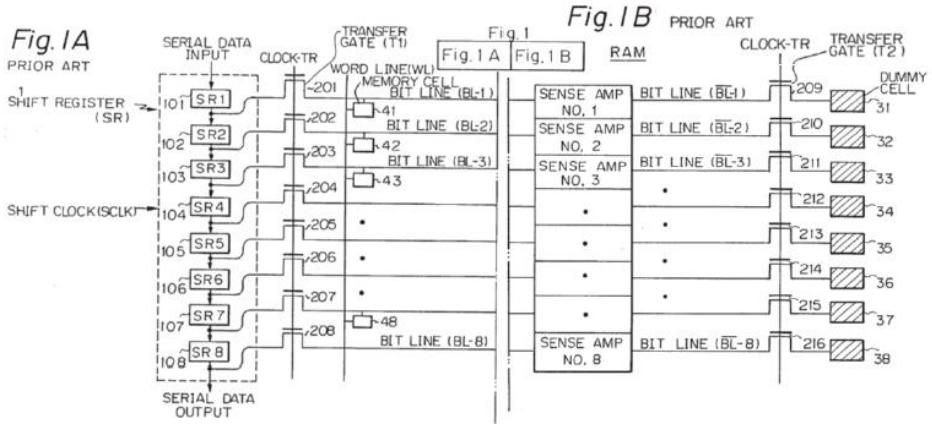
2. Obviousness of Claims 1–6 and 17–19 over Ogawa '577 (Ex. 1003), Ogawa '045 (Ex. 1005), and JP '832 (Ex. 1006)

Petitioner contends that Ogawa '577 (Ex. 1003), Ogawa '045 and JP '832 render obvious claims 1–6 and 17–19. Pet. 13–16. Petitioner relies on the Murphy declaration (Ex. 1004) and provides claim charts showing the claim limitations and the corresponding disclosure in Ogawa '577 (Pet. 13–37). Petitioner's analysis of the challenged claims also relies on Ogawa '045 and JP '832 to support its contentions that the references render claims 1–6 and 17–19 obvious. Pet. 10–12; 24–25; 32.

a. Analysis

With respect to claims 1–6, Petitioner provides claim charts and the Murphy declaration in support of the teachings that the disclosure in Ogawa '045 (Ex. 1005) teaches the common technique of using a sense amplifier on a bit line to write data stored in a shift register to either BL or $\overline{BL}$. Pet. 24–25; Ex. 1005, 3:40–65. Petitioner contends that the combination of the disclosure in Ogawa '577 with the techniques known to one of ordinary skill in the art disclosed in Ogawa '045 and JP '832 render claims 1–6 and 17–19 obvious. Pet. 24–25; 32–33; 34–36. Ogawa '045 and JP '832 are by the same inventor in the same field as Ogawa '577.

Ogawa '045 teaches a semiconductor memory device using RAM, a shift register and sense amplifiers arranged in the center of the RAM for Figures 1A and 1B of Ogawa '045, shown below.



Figures 1A and1B depict a schematic of prior art VRAM (video RAM) that uses shift register (SR) to write to BL-2 or $\overline{BL-2}$ via sense amplifiers (Sense Amp No. 2). Ex. 1005, 3:40–65. Combining the use of sense amplifiers in Ogawa '045 with the disclosure of Ogawa '577, Petitioner contends that Ogawa '045 teaches the technique of using sense amplifiers 101, 102, . . . 10n disclosed in Figure 2 of Ogawa '577 to read and write to the memory array to both BL and $\overline{BL}$. Pet. 24–25.

With respect to claims 17 and 18, Petitioner provides claim charts and analysis showing that Ogawa'577 and Ogawa '045 render claim 17 obvious. Pet. 28-33. Petitioner also provides claim charts and argument that Ogawa '577 (in combination with Ogawa '045) and JP '832 render the limitations of claims 18 and 19 obvious. Pet. 28–37.

JP '832 relates to random access memory (RAM) equipped with a shift register for high-speed reading and writing. Ex. 1006, 8. Figure 1 of JP '832 is shown below.

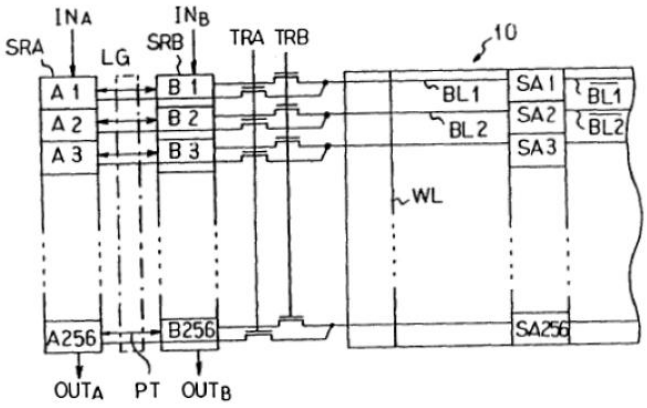


Figure 1 of JP ’832 shows a block diagram of open-bit-line RAM (10) with two shift registers, SRA and SRB. Ex. 1006, 8–9. JP ’832 discloses a video RAM comprising two shift registers SRA, SRB used to write a row of data into memory cells at the intersection of wordlines (WL) and bitlines (BL and $\overline{BL}$) of RAM memory array 10. Ex. 1006, 9–10. JP ’832 further discloses that reading data from one portion of the array, storing that data in the shift registers SRA and SRB, and writing that data in parallel to a different portion of the array or wordline (WL). Ex. 1006, 10–11.

Specifically, JP ’832 discloses writing via the shift registers, SRA and SRB, from one wordline to a new wordline in array 10. Ex. 1006, Fig. 6. Figure 6 of JP ’832 is shown below.

Figure 6

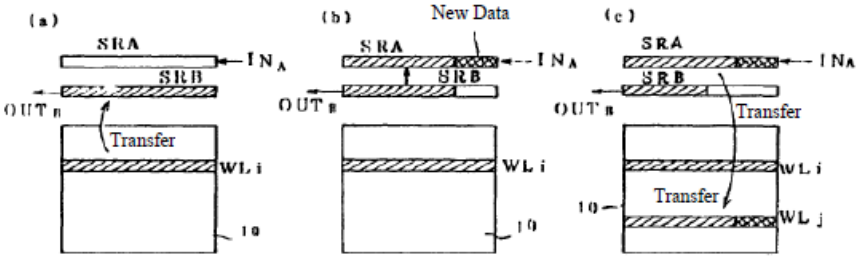


Figure 6 depicts shift registers SRA and SRB being used to transfer data from cells in a selected row WLi in memory array 10, to different cells in the selected row

WLj in memory array 10 along with New Data inserted in a portion of shift register A. Ex. 1006, 10–11.

Petitioner contends that the block data transfer in JP '832, in combination with the scroll display operation disclosed in Ogawa '577, discloses the limitations of dependent claims 18 and 19, which require writing the data via the master sense amplifiers to different memory cells in the selected row. Pet. 33–38. Petitioner also provides claim charts and citations to the Murphy declaration (Ex. 1004 ¶¶ 38–39) in support of its argument that JP '832, Ogawa '577 and Ogawa '045 disclose the limitations of claims 18 and 19.

Patent Owner contends that Petitioner fails to establish a prima facie case of obviousness for claims 1–6 and 17–19 because the Petition contains no separate sections addressing obviousness. Prelim. Resp. 26. Patent Owner further contends that Petitioner's arguments are confusing and incomplete in that they conflate arguments for obviousness and anticipation, failing to articulate sufficient reasoning with rational underpinnings to support the legal conclusion of obviousness. Prelim. Resp. 25–28.

We disagree with Patent Owner. Petitioner provides claim charts and argument stating what one of ordinary skill in the art would understand with respect to the disclosures in Ogawa '577, Ogawa '045, and JP '832 for each limitation of claims 1–6 and 17–19. Pet. 13–38. In addition, Petitioner cites the Murphy declaration in support of the understanding of one of ordinary skill in the art with respect to the cited references. Pet. 28–38 (citing Ex. 1004 ¶¶ 20, 26, 27, 32–36, 38, and 39). Contrary to the case cited by Patent Owner (Prelim. Resp. 26–27), i.e., *CailCopy, Inc. v. VerintAms., Inc*., IPR2013-00486, (PTAB Feb. 5, 2013) (Paper 11), Petitioner in the present case provides sufficient testimony and argument discussing what the cited prior art discloses to one of ordinary skill in the

art. *See, e.g.*, Pet. 19–25. Thus, based on the record before us, Petitioner has provided reasoning, with rational underpinning, in support of its contentions to demonstrate a reasonable likelihood that it would prevail in showing that claims 1–6 and 17–19 would have been obvious over the cited references.

Based on the record before us, Petitioner has demonstrated a reasonable likelihood that it will prevail in showing claims 1–6 and 17–19 would have been obvious over Ogawa '577 (Ex. 1003), Ogawa '045 (Ex. 1005) and JP '832 (Ex. 1006).

3. Anticipation of Claims 7–11 by JP '832 (Ex. 1006)

Petitioner asserts that JP '832 anticipates claims 7–11 of the '819 patent. Pet 30–44. JP '832 is the Japanese priority application corresponding to Ogawa '577. Pet. 34. Petitioner relies on the same argument presented above for claim 1, limitation [1i], to show that JP '832 discloses inherently using sense amplifiers to write data to the left and right sides of the memory array shown in Figure 1 of JP '832 as required in independent claim 7 (writing of said data through said master sense amplifiers to a second said row in said array). Pet 44–50 (discussing claim limitation 7[i]). Specifically, Petitioner argues that it was common practice based on the open bit line architecture of Figure 1 of JP '832 for sense amplifiers to be used to write data to both sides of the memory array in Figure 1 of JP '832. Pet. 46.

For the reasons discussed above with respect to claim 1, we are not persuaded that Petitioner has shown that JP '832 discloses necessarily that sense amplifiers are used to write data to the left and right sides of the memory array shown in Figure 1 of JP '832 as recited in claim 7. Pet. 44. Petitioner has not shown that "common practice" of one of ordinary skill in the art means that data

written from shift registers SRA and SRB of JP ’832 are written necessarily through sense amplifiers (SA1, SA2, etc.) shown in Figure 1 of JP ’832. Pet. 50.

Based on the foregoing, Petitioner has not shown a reasonable likelihood that it will prevail as to claims 7–11 being anticipated by Ogawa ’577.

4. Obviousness of Claims 7–11 over JP ’832 (Ex. 1006), Ogawa ’577 (Ex. 1003), and Ogawa ’045 (Ex. 1005)

Petitioner contends that JP ’832, Ogawa ’045 and Ogawa ’577 render claims 7–11 obvious. Petitioner provides claim charts showing the claim limitations and the corresponding disclosure in JP ’832. Pet. 38–59. Petitioner also provides argument and discussion regarding the disclosures of Ogawa ’045 and Ogawa ’577 and citations to the Murphy declaration (Ex. 1004 ¶¶ 40–84) supporting the argument that the cited references render claims 7–11 obvious. Pet. 38–60.

With respect to claims 7–11 and based on the present record, we disagree with Patent Owner’s contention that Petitioner fails to articulate sufficient reasoning with rational underpinnings to support the legal conclusion of obviousness. Prelim. Resp. 24–30. Similar to the discussion above, Petitioner has provided sufficient testimony in the Murphy declaration (Ex. 1004 ¶¶ 40–84) and argument and discussion in the Petition stating what the cited prior art discloses to an ordinarily skilled artisan. Pet. 38–60. Thus, we find that Petitioner’s argument and evidence on the present record provide sufficient reasoning with rationale underpinnings in support of their contentions that claims 7–11 would have been rendered obvious by the combination JP ’832, Ogawa ’577, and Ogawa ’045.

Based on the foregoing, Petitioner has demonstrated a reasonable likelihood that it will prevail in showing claims 7–11 would have been obvious over JP ’832 (Ex. 1006), Ogawa ’577 (Ex. 1003), and Ogawa ’045 (Ex. 1005).

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the petition establishes a reasonable likelihood that Petitioner will prevail in showing the unpatentability of each of claims 1-11 and 17-19 of the '819 Patent.

The Board has not yet made a final determination of the patentability of these claims or the construction of any claim term.

IV. ORDER

For the reasons given, it is

ORDERED that *inter partes* review is instituted as to claims 1–11 and 17–19 on the ground that the claims are unpatentable under 35 U.S.C. § 103(a) as rendered obvious by Ogawa '577, Ogawa '45, and JP '832;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '819 patent is hereby instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial;

FURTHER ORDERED that all grounds not listed in the Conclusion are *denied*, and no ground other than those specifically granted above is authorized for the *inter partes* review as to claims 1–11 and 17–19 of the '819 patent.

PETITIONER:

Gianni Minutolli
Gianni.minutoli@dlapiper.com

Kevin Hamilton
Kevin.hamilton@dlapiper.com

PATENT OWNER:

Lori Gordon
Lgordon-PTAB@skgf.com

Michael Specht
Mspecht-PTAB@skgf.com

Omar Amin
Oamin-PTAB@skgf.com