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Paper 12
Entered: September 25, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HARMONIC, INC.
Petitioner

v.

AVID TECHNOLOGY, INC.
Patent Owner

Case IPR2013-00252
U.S. Patent No. 5,495,291

Before JONI Y. CHANG, MICHAEL R. ZECHER, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

ZECHER, *Administrative Patent Judge*

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Harmonic, Inc. ("Harmonic") filed a petition ("Pet.") requesting *inter partes* review of claims 1-20 of U.S. Patent No. 5,495,291 ("the '291 patent"). Paper 1. Patent owner, Avid Technology, Inc. ("Avid"), filed a preliminary response ("Prelim. Resp."). Paper 10. We have jurisdiction under 35 U.S.C. § 314.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides:

> THRESHOLD—The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

For the reasons set forth below, we conclude that the information presented in the petition establishes that there is a reasonable likelihood that Harmonic will prevail in challenging claims 1-16 as unpatentable. However, we conclude that the information presented in the petition does not establish that there is a reasonable likelihood that Harmonic will prevail in challenging claims 17-20 as unpatentable. Pursuant to 35 U.S.C. § 314, we hereby authorize an *inter partes* review to be instituted only as to claims 1-16 of the '291 patent.

A. Related Matters

Harmonic indicates that the ’291 patent was asserted against it in *Avid Technology, Inc. v. Harmonic, Inc.*, Case No. 1:12-cv-00627-GMS, filed in the U.S. District Court for the District of Delaware. Paper 4.

B. The Invention of the ’291 Patent (Ex. 1001)

The invention of the ’291 patent relates to decompressing compressed video data. Ex. 1001, 1:9-12. According to the ’291 patent, video data typically includes video and audio data contained in a stored video program. Ex. 1001, 1:13-15. However, other data such as text and graphics data also may be included in the video data. Ex. 1001, 1:15-18.

The ’291 patent discloses a known compression format sponsored by the Motion Picture Expert Group (“MPEG”). Ex. 1001, 1:28-29. MPEG compression is predicated on the notion that, from one frame of video data to the next, there are comparatively few changes, even when objects or persons are in motion. Ex. 1001, 1:33-35. Therefore, it is not necessary to store all of the video data contained in each frame. Ex. 1001, 1:35-37. Rather, after a base frame has been stored, each successive frame can be recreated by storing only the video data that describes objects or persons that either have changed or moved. Ex. 1001, 1:37-40. Periodically, a complete frame of video data must be stored to re-initialize the process. Ex. 1001, 1:40-42. The ’291 patent discloses that this type of data compression is called motion compensation. Ex. 1001, 1:42-43.

Figure 2 of the '291 patent illustrates a known architecture for decoding MEPG video data streams. Ex. 1001, 2:12-13; 3:56-57. Figure 2 is reproduced below:

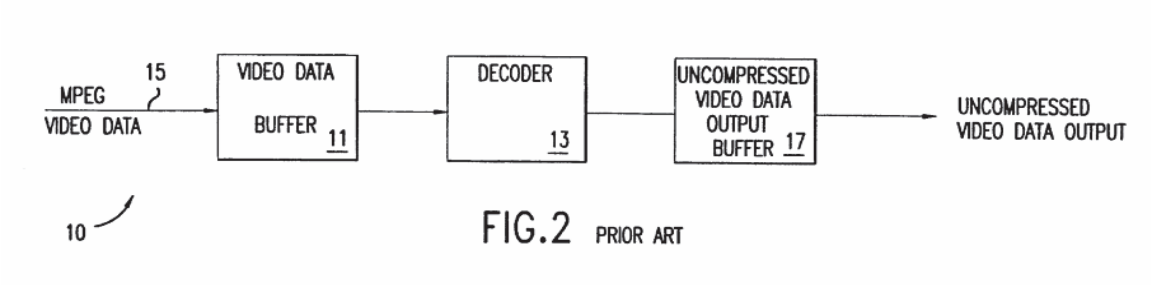

FIG.2 PRIOR ART

Figure 2 illustrates a prior art system for decompressing video data.

The decompression system 10 includes compressed video data buffer 11, decoder 13, and decompressed video data buffer 17. Ex. 1001, 2:13-15. An input bus 15 provides a stream of compressed MPEG video data to buffer 11. Ex. 1001, 2:15-16. The input bus 15 also provides video data at a fixed rate, i.e., a period of time elapses before enough video data is stored in buffer 11 for decoder 13 to begin decompressing the video data. Ex. 1001, 2:17-19.

A latency time—commonly referred to as a buffer filling latency time—exists before enough MPEG video data enters buffer 11 for decoder 13 to begin decompression. Ex. 1001, 2:20-22. An even longer latency time—commonly referred to as a reordering latency time—occurs due to the nature of the MPEG video data. Ex. 1001, 2:22-24, 29-31. The reordering latency time exists because the system must receive and decompress I-frames and P-frames before it can decompress B-frames. Ex. 1001, 2:27-29.

The effect of the reordering latency time is noticeable every time a new video program begins. Ex. 1001, 2:32-33.

The reordering latency time and the buffer latency time together result in the system generating several blank frames between the old and new video programs while the new video program is decompressed sufficiently for display. Ex. 1001, 2:33-37. These blank frames are undesirable. Ex. 1001, 2:39-40. According to the '291 patent, the disclosed invention solves this problem at an acceptable cost. Ex.1001, 2:41-42.

Figure 3 of the '291 patent illustrates the preferred embodiment of the disclosed invention. Ex. 1001, 3:58-59, 66-67. Figure 3 is reproduced below:

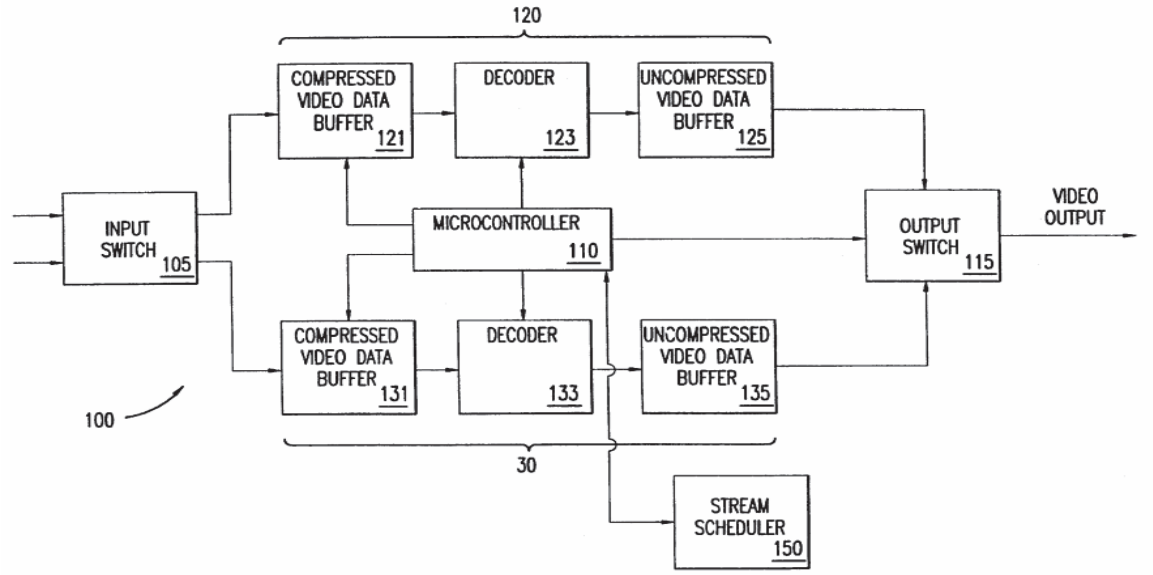

FIG.3

Figure 3 illustrates decompression system 100.

The decompression system 100 includes input switch 105, first and second decompression circuits 120 and 130, output switch 115, and microcontroller 110. Ex. 1001, 3:67-4:6. The first and second compression circuits 120 and 130 include, respectively, compressed video data buffers 121 and 131, first and second decoders 123 and 133, and decompressed video data buffers 125 and 135. *Id*. Stream scheduler 150 is coupled to microcontroller 110. Ex. 1001, 4:6.

C. Illustrative Claim

Claims 1, 9, and 17 are independent claims. Claims 2-8 directly or indirectly depend from independent claim 1, claims 10-16 directly or indirectly depend from independent claim 9, and claims 18-20 directly depend from independent claim 17. Independent claim 1 is illustrative of the invention of the '291 patent and is reproduced below:

> 1. A system for decompressing video data streams and for providing continuous video data output, the system comprising:
>
> an input switch coupled to a plurality of compressed video data input lines, the switch capable of selecting input lines and capable of controlling the video data flow rate of the selected input lines;
>
> a plurality of decompression modules coupled to the input switch for decompressing compressed video data received from the input switch and storing decompressed video data;
>
> an output switch coupled to the decompression modules, the output switch coupling only one of the decompression modules to an output bus at any time; and
>
> a controller coupled to the input switch, the decompression modules, and the output switch for selecting

> which decompression module will receive video data at a first predefined rate, the decompression module receiving video data at the first predefined rate also being coupled to the output bus by the output switch.

Ex. 1001, Claims—6:25-45.

D. Prior Art Relied Upon

Harmonic relies upon the following prior art references:

Allen	US 5,381,145	Jan. 10, 1995 (filed Feb. 10, 1993)	Ex. 1005
Hang	US 5,115,309	May 19, 1992	Ex. 1006
Paik	US 5,216,503	June 1, 1993	Ex. 1007
Haskell	US 5,159,447	Oct. 27, 1992	Ex. 1008
Rossmere	US 5,508,940	Apr. 16, 1996 (filed Feb. 14, 1994)	Ex. 1009

Admitted Prior Art—the background section of the '291 patent (Ex. 1001, 1:9-2:43; Fig. 2), certain disclosures in the detailed description section of the '291 patent (e.g., Ex. 1001, 4:6-8, 26-29), and the prosecution history of the '291 patent (Ex. 1004) (hereinafter "APA").

E. Alleged Grounds of Unpatentability

Harmonic challenges claims 1-20 of the '291 patent based on the alleged grounds of unpatentability set forth in the table below.

Reference(s)	**Basis**	**Claims Challenged**
APA	§ 103(a)	1-20
APA and Hang	§ 103(a)	1-20
Paik and Rossmere	§ 103(a)	1-10
Paik , Rossmere, and Haskell	§ 103(a)	11-16
Paik	§ 102(b)	17-20
Haskell and Rossmere	§ 103(a)	1-16
Haskell	§ 102(b)	17-20

II. CLAIM CONSTRUCTION

Consistent with the statute and legislative history of the Leahy-Smith America Invents Act, Pub. L. 112-29, 125 Stat. 284, 329 (2011), the Board construes claims by applying the broadest reasonable interpretation in light of the specification. 37 C.F.R. § 42.100(b); *see also* Office Patent Trial Practice Guide, 77 *Fed. Reg.* 48756, 48766 (Aug. 14, 2012). There is a "heavy presumption" that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). However, a "claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history." *Id*. "Although an inventor is indeed free to define the specific terms used to describe his or her invention, this must be done with reasonable clarity, deliberateness, and precision." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

A. "For providing continuous video data output" (Claim 1) and "For providing continuous decompressed video data to an ouput" (Claim 17)

Harmonic contends that the preambles of independent claims 1 and 17 amount to statements of intended use and, therefore, are not entitled to patentable weight. Pet. 11-12. In response, Avid contends that the preambles of independent claims 1 and 17 define the required structure of

the video data output and, therefore, are entitled to patentable weight. Prelim. Resp. 4-6. In particular, Avid argues that intended purpose of the invention of the '291 patent is to provide a decompression system with a continuous, uninterrupted decompressed video data output stream. *Id*. at 5 (citing to Ex. 1001, Title, Abstract). Avid then asserts that the preamble of independent claim 1 is needed to breathe life and meaning into the characteristics of the video output flowing from the claimed "output switch." *Id*. at 6. Avid implies that the same analysis is applicable to the preamble of independent claim 17. *Id*.

In considering whether a preamble limits a claim, the preamble is analyzed to ascertain whether it states a necessary and defining aspect of the invention or is simply an introduction to the general field of the claim. *On Demand Machine Corp. v. Ingram Indus., Inc.*, 442 F.3d 1331, 1343 (Fed. Cir. 2006); *see also Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 952 (Fed. Cir. 2006). A preamble is construed as a limitation "if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.,* 289 F.3d 801, 808 (Fed. Cir. 2002) (quoting *Pitney Bowes, Inc. v. Hewlett-Packard Co.,* 182 F.3d 1298, 1305 (Fed. Cir. 1999)). However, a preamble is not limiting "'where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.'" *Catalina Mktg.,* 289 F.3d at 808 (quoting *Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997)); *see also Symantec Corp. v. Computer Assocs. Int'l Inc.*, 522 F.3d 1279, 1288 (Fed. Cir. 2008).

In this case, the issue turns on whether "for providing continuous video data output" recited in the preamble of independent claim 1, and "for providing continuous decompressed video data to an output" recited in the preamble of independent claim 17, each state a necessary and defining aspect of the invention disclosed in the '291 patent. To resolve this issue, we look to the specification of the '291 patent because the words of a claim must be interpreted as would be understood by one with ordinary skill in the art upon reading the entire disclosure. *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004).

We agree with Avid that both the Title and Abstract of the '291 patent disclose a decompression system with a continuous, uninterrupted decompressed video data output stream. Ex. 1001, Title, Abstract. A review of the specification of the '291 patent provides additional context. The specification of the '291 patent discloses that "[o]utput switch 115 would be instructed by microcontroller 110 to switch the output to decompression circuit 130 as the output from decompression circuit 120 ends, insuring [sic] a continuous generation of decompressed video data without any blank frames between video streams." Ex. 1001, 5:15-19. When describing the relative rates of video data transmission through the first and second decompression circuits (120 and 130), the specification of the '291 patent discloses that "[t]his sequential process continues until all video data streams provided as input have been decompressed and provided as output in a continuous data stream." Ex. 1001, 5:62-65. These cited disclosures in the '291 patent describe a continuous output as a fundamental characteristic of

the components of the "system for decompressing video data streams" recited in the body of independent claim 1, and the method steps recited in the body of independent claim 17. As a result, we conclude that the aforementioned recitations in the preambles of independent claims 1 and 17 are entitled to patentable weight because they each state a necessary and defining aspect of the invention disclosed in the '291 patent.

B. "Input switch . . . capable of controlling the video flow rate" (Claim 1)

Harmonic contends that the claim phrase an "input switch . . . capable of controlling the video flow rate" should be construed as "controlling the time, duration, and rate at which video data flows into the selected input lines, and includes some level of control beyond simply turning flow on or off." Pet. 12. To support its claim construction, Harmonic directs us to the declaration of Dr. Kenneth A. Zeger. *Id*. (citing to Ex. 1002 ¶¶ 38-39). The cited paragraphs in the declaration of Dr. Zeger refer to multiple disclosures in the specification of the '291 that support Harmonic's claim construction. *See, e.g.*, Ex. 1001, 4:38-52; 5:8-10, 19-21, 43-46. Avid does not dispute Harmonic's claim construction with respect to the claim phrase an "input switch . . . capable of controlling the video flow rate." For purposes of this decision, we adopt Harmonic's claim construction because it is consistent with the specification of the '291 patent.

C. "Lines" (Claims 1 and 9)

Harmonic contends that the claim term "lines" should be construed as "any means for conducting the claimed 'data streams,' including physical lines (e.g., conductive wires) or otherwise." Pet. 12. To support its claim construction, Harmonic directs us to the declaration of Dr. Zeger. *Id*. (citing to Ex. 1002 ¶ 40). The cited paragraph in the declaration of Dr. Zeger does not refer to a particular disclosure in the specification of the '291 that supports Harmonic's claim construction. Avid does not dispute Harmonic's claim construction with respect to the claim term "lines."

Upon reviewing the specification of the '291 patent, we do not find an explicit definition for the claim term "lines." Therefore, we refer to its ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc*., 504 F.3d 1249, 1257 (Fed. Cir. 2007). For purposes of this decision, we adopt Harmonic's claim construction because it is consistent with the ordinary and customary meaning of "lines" as would be understood by one with ordinary skill in the art in the context of the '291 patent.

D. "Buffer"(Claims 2 and 3)

Harmonic contends that the claim term "buffer" should be construed as "a means for data storage." Pet. 13. To support is claim construction, Harmonic directs us to a particular disclosure in the specification of the '291 patent, as well as the declaration of Dr. Zeger. *Id*. (citing to Ex. 1001, 4:31-37; Ex. 1002 ¶ 41). The cited paragraph in the declaration of Dr. Zeger

simply reiterates the disclosure in the specification of the ’291 patent already cited by Harmonic. Avid does not dispute Harmonic’s claim construction with respect to the claim term “buffer.”

We agree with Harmonic that a “buffer” stores data, but it is a temporary data storage. In support of our position, we note that the Microsoft Computer Dictionary 76, 5th ed. (2002) defines a “buffer” as “a region of memory reserved for use as an intermediate repository in which data is temporarily held while waiting to be transferred between two locations or devices.” Therefore, for purposes of this decision, we construe the claim term “buffer” as “a temporary means for data storage.”

E. “Switch” (Claims 1, 4, 9, 15, and 16)

Harmonic contends that one with ordinary skill in the art would have understood that the term “switch” generally refers to a device/assembly that provides a routing or selecting function in electronic circuitry. Pet. 13. Harmonic then asserts that the claim term “switch” should be construed as “a device or assembly for routing or selecting a data stream.” *Id*. Harmonic argues that a switch may be coupled directly or indirectly to another component, and may include a multiplexer, demultiplexer, or combination thereof. *Id*. (citing to Ex. 1002 ¶¶ 42-44). The cited paragraphs in the declaration of Dr. Zeger do not refer to a particular disclosure in the specification of the ’291 that supports Harmonic’s claim construction. Avid does not dispute Harmonic’s claim construction with respect to the claim term “switch.”

Upon reviewing the specification of the ’291 patent, we do not find an explicit definition for the claim term “switch.” Therefore, we refer to its ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *Translogic*, 504 F.3d at 1257. For purposes of this decision, we adopt Harmonic’s claim construction because it is consistent with the ordinary and customary meaning of a “switch” as would be understood by one with ordinary skill in the art in the context of the ‘291 patent.

F. “Controller” (Claims 1, 4, 9, 11, 15, and 16)

Harmonic contends that the specification of the ’291 patent does not recite the term “controller,” but instead identifies microcontroller 100, e.g., a Motorola 68331 microcontroller. Pet. 13 (citing to Ex. 1001, 4:6-9). Based on that disclosure, Harmonic contends that the claim term “controller” should be construed “to include a component or subsystem that cause[s], directly or indirectly, aspects of operation of a device.” Pet. 13-14. Harmonic argues that a controller may include the identified Motorola 68331 microcontroller, as well as other commercially available controller components. *Id*. at 14 (citing to Ex. 1002 ¶ 45). The cited paragraph in the declaration of Dr. Zeger simply reiterates the disclosure in the specification of the ’291 that identifies microcontroller 110 as a Motorola 68331 microcontroller. Avid does not dispute Harmonic’s claim construction with respect to the claim term “controller.” For purposes of this decision, we

adopt Harmonic's claim construction because it is consistent with the specification of the '291 patent.

G. "Output bus" (Claims 1, 9, and 16)

Harmonic contends that the specification of the '291 patent does not set forth an explicit definition for the claim term "output bus." Pet. 14. However, Harmonic indicates that Figures 2 and 3 of the '291 patent provide a generic illustration of a video data output bus. *Id*. Based on those Figures, Harmonic contends that the claim term "output bus" should be construed to include "a video output or output path in a prior art known manner, consistent with the disclosure provided, e.g., in Figure 2 and 3 of the '291 patent." *Id*. (citing to Ex. 1001; Ex. 1002 ¶ 46). The cited paragraph in the declaration of Dr. Zeger merely refers to the example of an "output bus" illustrated in Figure 2 of the '291 patent. Avid does not dispute Harmonic's claim construction with respect to the claim term "output bus." For purposes of this decision, we adopt Harmonic's claim construction because it is consistent with the specification of the '291 patent.

H. "Predefined rate" (Claims 1 and 5-8)

Harmonic contends that the claim term "predefined rate" cannot be found in the specification of the '291 patent. Pet. 14. Harmonic also indicates that the specification of the '291 patent does not provide guidance as to a reference point for a rate determination, such as prior to compression or after compression. *Id*. Harmonic contends that the broadest reasonable

interpretation of the claim term "predefined rate" should not be "limited to any particular time of determining the rate." *Id*. (citing to Ex. 1002 ¶ 47). The cited paragraph in the declaration of Dr. Zeger construes the claim term "predefined rate" as "a rate determined at any time prior to the step presently being performed." Ex. 1002 ¶ 47. Avid does not dispute Dr. Zeger's claim construction with respect to the claim term "output bus." For purposes of this decision, we adopt Dr. Zeger's claim construction because it is consistent with the specification of the '291 patent.

I. "A plurality of compressed video data input lines" (Claim 1), "At least two compressed video data input lines" (Claim 9), and "A plurality of compressed video data streams (Claim 17)

Avid contends that the specification of the '291 patent explicitly defines these claim phrases as requiring that "each of the plurality of video data input lines or streams comprises different individual video programs." Prelim. Resp. 6. To support its claim construction, Avid directs us to a portion of the specification of the '291 patent that states:

> For purposes of this description a compressed video data stream can be comprised of a single video program or multiple video programs. *Different video data streams will therefore comprise different individual video programs.* The video data streams may be available simultaneously at the input of the present invention or they can be received at different times.

Id. at 6-7 (citing to Ex. 1001, 2:49-55 (emphasis added by Avid)). Avid argues that a plurality of video data input streams or lines each must include a different video program, which is in contrast with a single video program

that is separated into multiple streams for parallel processing. *Id*. at 7. We do not agree with Avid.

We must be careful not to read a particular embodiment appearing in the specification into the claim if the claim language is broader than the embodiment. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Here, we decline to adopt Avid's claim construction, as it would import limitations improperly from the specification of the '291 patent into the claims. The portion of the specification of the '291 patent relied upon by Avid is associated with a first preferred embodiment and does not constitute an explicit definition.

Upon reviewing the specification of the '291 patent in its entirety, we do not find an explicit definition that indicates a plurality of compressed video data input lines or streams each must include different video programs and, therefore, excludes separating a single video program into a plurality of compressed video data input lines or streams. In other words, a plurality of compressed video data input lines or streams should not be construed so narrowly as to preclude separating a single video program into multiple video data input lines or streams for parallel processing—the alleged point of novelty that distinguishes the invention of the '291 patent from the prior art. *See* Ex. 1004 at p. 0060. Accordingly, applying the broadest reasonable interpretation consistent with the specification of the '291 patent, a plurality of compressed video data input lines or streams may be construed as each including a portion of a single video program.

J. Remaining Claim Terms or Phrases[1]

All remaining claim terms or phrases recited in claims 1-20 are given their ordinary and customary meaning as would be understood by one with ordinary skill in the art, and need not be further construed at this time.

III. ANALYSIS

A. 35 U.S.C. § 103(a) Ground of Unpatentability—Combination of Haskell and Rossmere

Claims 1-16

Harmonic contends that claims 1-16 are unpatentable under 35 U.S.C. § 103(a) over the combination of Haskell and Rossmere. Pet. 43-52. In particular, Harmonic explains how the combination of Haskell and Rossmere allegedly teaches the claimed features recited in these claims, and

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[1] Harmonic contends that dependent claim 4 lacks antecedent basis for the claim terms "the first switch," "the second rate," and "the video data compression array" and, therefore, raises issues related to indefiniteness under 35 U.S.C. § 112, second paragraph. Pet. 14-15. However, a petitioner in an *inter partes* review may request to cancel as unpatentable 1 or more claims of a patent only on a ground of unpatentability that could be raised under § 102 or 103 and only on the basis of prior art consisting of patents or printed publications. *See* 35 U.S.C. § 311(b). For purposes of this decision, we address only those grounds of unpatentability asserted under §§ 102 and 103. In any event, the mere failure to provide antecedent bases for claim terms does not always render a claim indefinite. If the scope of a claim would be reasonably ascertainable by a person of ordinary skill in the art, then the claim is not indefinite. *See, e.g., Energizer Holdings Inc. v. Int'l Trade Comm'n*, 435 F.3d 1366, 1370 (Fed. Cir. 2006).

relies upon the Declaration of Dr. Zeger to support its positions. *Id*. We are persuaded by Harmonic's explanations and supporting evidence.

We begin our analysis with a general discussion of Haskell and Rossmere, followed by the positions taken by Harmonic with respect to independent claim 1, and then we turn to the arguments presented by Avid that are directed towards the combination of Haskell and Rossmere.

1. Haskell (Ex. 1008)

Haskell relates to avoiding encoder and decoder buffer overflow and underflow when transmitting an image over a variable bit-rate channel. Ex. 1008, 1:6-9. According to Haskell, the disclosed invention solves the problem of buffer overflow and underflow in a decoder when employing variable bit-rate channels for communicating encoded video images. Ex. 1008, 1:65-2:8.

Figure 2 of Haskell illustrates an encoding system that encodes a number of individual unencoded bit-streams and multiplexes these bit-streams into a single bit-stream. Ex. 1008, 2:56-59; 11:6-10. Figure 2 is reproduced below:

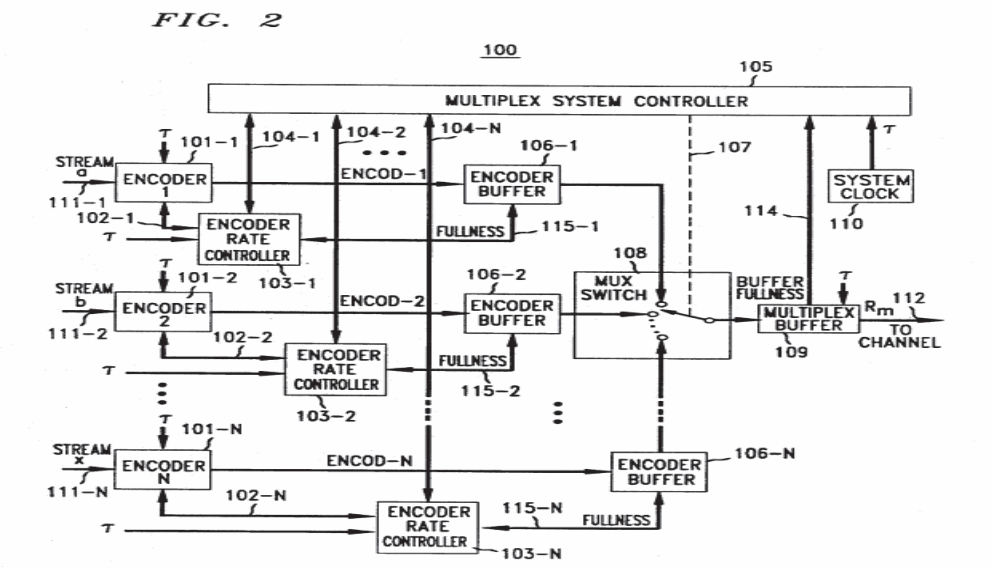

Figure 2 illustrates encoding system 100 wherein a number of individual unencoded bit streams 111-1 through 111-N are encoded and multiplexed into a single bit-stream 112 for transmission.

Haskell discloses that encoders 101-1 through 101-N each receives an individual unencoded bit-stream 111-1 through 111-N as an input. Ex. 1008, 11:67-12:1. Each of the individual unencoded bit-streams may be derived from a different source, e.g., video, audio, and data. Ex. 1008, 11:21-25. For purposes of this example, unencoded bit-stream 111-1 is designated as a video signal and unencoded bit-stream 111-2 is designated as an audio signal. Ex. 1008, 12:1-4. Encoders 101-1 through 101-N each encodes the type of data carried in the individual unencoded bit-stream supplied thereto and, subsequently, supplies as an output an encoded representation of that data. Ex. 1008, 12:4-10. Each of the encoders 101-1 through 101-N is associated with one of the encoder buffers 106-1 through 106-N. Ex. 1008, 12:10-12. Each of the encoder buffers 106-1 through 106-

N stores the encoded bit-streams supplied from the corresponding encoders. Ex. 1008, 12:12-15. Each of the encoder buffers 106-1 through 106-N supplies the stored encoded bit-streams in a first in, first out fashion through multiplexer switch 108 to multiplex buffer 108 prior to transmission by a channel. Ex. 1008, 12:15-19.

Figure 3 of Haskell illustrates a demultiplexer and decoder system. Ex. 1008, 2:60-61; 13:35-36. Figure 3 of Haskell is reproduced below:

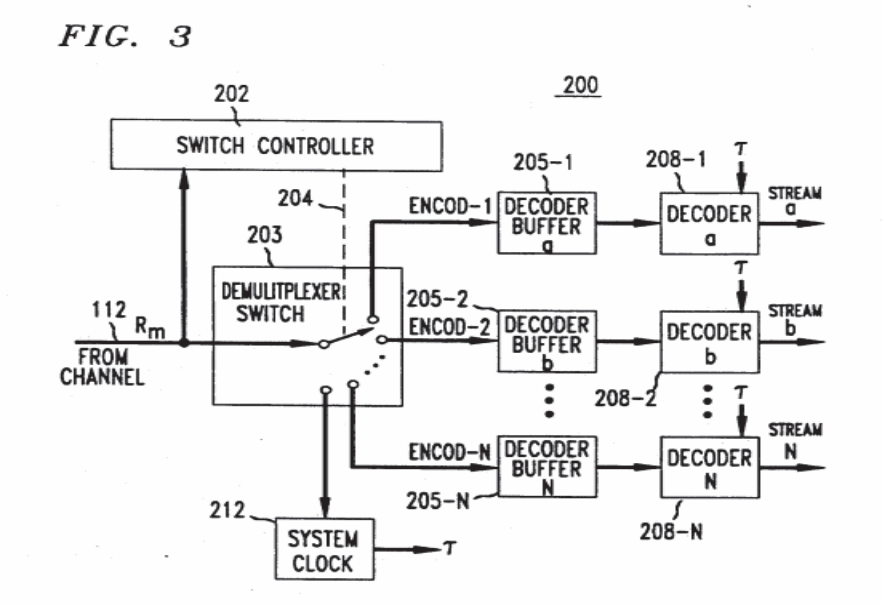

Figure 3 illustrates a demultiplexer and decoder system 200 that corresponds to the encoding system 100 illustrated in Figure 2.

Haskell discloses that switch controller 202 identifies the packets of multiplex data stream 112 that are incoming from the channel. Ex. 1008, 13:35-39. Demultiplexer 203 then switches the packets to one of the corresponding decoder buffers 205-1 through 205-N. Ex. 1008, 13:39-41. The packets remain in decoder buffers 205 until their respective decoders

208-1 through 208-N are ready to decode them. Ex. 1008, 13:46-48. Haskell discloses that, because the decoder buffers only have a finite capacity, it is the responsibility of encoder 100 (illustrated in Figure 2) to ensure that they do not overflow or underflow. Ex. 1008, 14:12-14.

2. Rossmere (Ex. 1009)

Rossmere discloses a multimedia random access audio/video editing system that allows users to configure the editing system to suit their needs. Ex. 1009, 1:34-37. The invention disclosed in Rossmere includes triple transfer buffers, i.e., a present buffer, a past buffer, and a future buffer, which ensure that there is sufficient video and audio material in the present buffers to play, such that a prospective user will not perceive discontinuities in either the audio or video channel outputs. Ex. 1009, 2:40-46. Figure 3a of Rossmere illustrates the circuit components of the disclosed invention. Ex. 1009, 3:46-47; 6:62-64. Figure 3a is reproduced below:

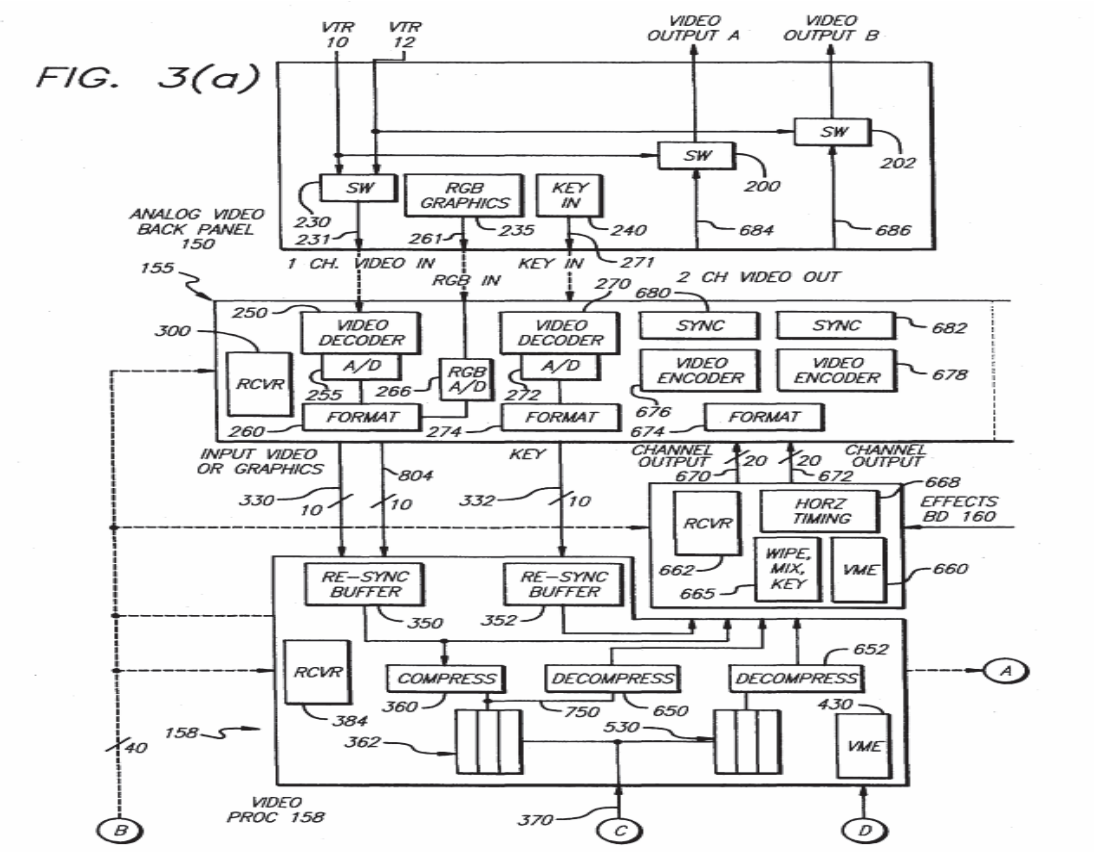

Figure 3a illustrates the primary components of the main control unit 60 illustrated in Figure 1.

The invention disclosed in Rossmere provides the ability to bypass the main control unit 60 by routing signals selectively from video tape recorder ("VTR") 10 and VTR 12 directly through switches 200 and 202 to the video outputs A (67 illustrated in Figure 1) and B (66 illustrated in Figure 1). Ex. 1009, 7:17-21. Rossmere also discloses that switches 200 and 202 are coupled, respectively, to the video outputs provided over lines 684 and 686. Ex. 1009, 11:26-28. As discussed above, the selection of switches 200 and

202 provide output along lines 684 and 686, or direct output from the video inputs provided by VTR 10 and VTR 12. Ex. 1009, 11:28-32.

3. Harmonic's Findings and Conclusions

Harmonic explains how Haskell teaches all the claimed features recited in independent claim 1, except an "output switch" for selecting between the different output streams. Pet. 44-45. Harmonic argues that, while Haskell does not disclose explicitly an "output switch," it would have been obvious to one of ordinary skill in the art to incorporate an output switch into Haskell's decompression system because it would provide a means for selection between a plurality of outputs of different compressed data streams. *Id*. at 45-46. In addition, Harmonic argues that, to the extent that it would not have been obvious to incorporate an output switch into Haskell's decompression system, such a component may be found in prior art decompression systems as being employed for selecting among data output streams. *Id*. at 46. According to Harmonic, Rossmere serves as one example of a decompression system that uses an output switch. *Id*. at 47. In response to Harmonic's alleged ground of unpatentability based on the combination of Haskell and Rossmere, Avid presents a number of arguments. We will address each argument in turn.

4. Avid's Contentions

Avid contends that Haskell addresses buffer problems that result from streaming a video program or other data over a variable rate transmission channel. Prelim. Resp. 31-32. Avid argues that Haskell is not concerned with the continuous output of multiple video transmissions and, therefore,

has no need for an output switch. *Id*. at 32. Avid's argument is predicated on the notion that Haskell is non-analogous to the invention of the '291 patent. We find Avid's argument unpersuasive.

Two criteria have evolved for determining whether prior art is analogous: "(1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved." *In re Clay*, 966 F.2d 656, 658-59 (Fed. Cir. 1992) (citing *In re Deminski*, 796 F.2d 436, 442 (Fed. Cir. 1986); *In re Wood*, 599 F.2d 1032, 1036 (CCPA 1979)). "A reference is reasonably pertinent if . . . it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem." *Id*. at 659.

The invention of the '291 patent solves the problem of blank frames between video lines or streams by ensuring a continuous generation of decompressed video data output. Ex. 1001, 5:15-19. As discussed above, Haskell solves the problem of buffer overflow and underflow in a decoder when employing variable bit-rate channels for communicating encoded video images. Ex. 1008, 1:65-2:8. We conclude that one with ordinary skill in the art would have recognized that Haskell's disclosure of preventing buffer overflow and underflow logically would commend itself to the patentee's attention when considering how to output decompressed video data continuously. Given that Haskell is analogous to the invention of the '291 patent, we are not persuaded by Avid's argument that Haskell has no

need for an output switch. Avid does not provide a sufficient or credible explanation as to why it would not have been obvious for one with ordinary skill in the art to incorporate an output switch into Haskell's system.

Next, Avid contends that the position taken by Harmonic—namely that one with ordinary skill in the art would have found it obvious to incorporate an output switch into Haskell's system—is based on a misleading interpretation of Figures 1 and 3 illustrated in Haskell. Prelim. Resp. 32-35. In particular, Avid argues that Dr. Zeger testifies that Figure 3 of Haskell shows a portion of the complete system shown in Figure 1 of Haskell, and that Figure 1 of Haskell shows that multiple output streams illustrated in Figure 3 of Haskell ultimately are combined into a single output. *Id*. at 32 (citing to 1002 ¶ 267). Avid asserts that contrary to Dr. Zeger's testimony, the multiple input embodiment illustrated in Figure 3 of Haskell is not a truncated portion of the decoder unit illustrated in Figure 1 of Haskell. *Id*. at 35.

The relevant portions of Dr. Zeger's testimony are reproduced below:

> While Haskell illustrates a number of different output data streams following decompression (see, e.g., Ex. 1008 at Fig. 2, Stream a, b, . . . N; Fig. 4), Haskell does not explicitly illustrate a particular "output switch" for selecting between the different output streams. It is my opinion, however, that the use of such an output selection means in [the] system of Haskell would be communicated and understood by one of ordinary skill as an obviously included component to the Haskell system. *One reason, for example, is that while the decoder unit 200 of Fig. 3 is truncated with respect to the output streams, Fig. 1 of Haskell illustrates a single output from decoder unit 45*. Additionally, one of skill would ordinarily understand that

> where a decompression system shows a plurality of outputs of different decompressed data streams, some sort of means for selecting between the outputs, and therefore making use of the system data streams, would normally, if not necessarily, be employed. A commonly employed selection means at the time would have included some sort of switch. A switch as a selection means option would have been particularly apparent to one of skill in view of the fact that the Haskell system illustrates use of switches (e.g., Mux switch 108, demultiplexer switch 203) upstream of the data decompression.

Ex. 1002 ¶ 267 (emphasis added). Contrary to Avid's argument, Dr. Zeger does not testify that the multiple input embodiment illustrated in Figure 3 of Haskell is a truncated portion of the decoder unit illustrated in Figure 1 of Haskell. Instead, Dr. Zeger's testifies that the decoder unit 200 illustrated in Figure 3 of Haskell is truncated with respect to the output streams—not with respect to the decoder unit illustrated in Figure 1 of Haskell. Moreover, Dr. Zeger simply relies upon the single output from decoder unit 45 illustrated in Figure 1 of Haskell as an example of an output selection taught by Haskell. In our view, that example supports Harmonic's position that while Figures 2 and 3 of Haskell do not include an output switch, it would have been obvious to one with ordinary skill in the art to incorporate an output switch—albeit disclosed in another embodiment of Haskell—into the embodiment illustrated in Figures 2 and 3 of Haskell. *See* Pet. 45-46.

Avid further contends that there is no reason to combine the multiple output streams illustrated in Figure 3 of Haskell into a single output. Prelim. Resp. 35. Avid generally alleges that the intended purpose of Haskell is to recreate the multiple input signals that are derived from different sources,

e.g., video, audio, and data sources, at the output of the system by compensating for the variable bit-rate transmission channel. *Id*. at 35-36. Avid also argues that, absent impermissible hindsight reconstruction, there simply is no reason that one with ordinary skill in the art would have contemplated adding an output switch to Haskell's system in order to generate a single continuous output stream from the multiple output streams illustrated in Figure 3 of Haskell. Prelim. Resp. 35-36. In summary, Avid makes two separate arguments: (1) there is no reason to modify Haskell with an output switch or, alternatively, with the teachings of Rossmere; and (2) modifying Haskell's system with an output switch would change Haskell's principle of operation, or render Haskell inoperable for its intended purpose. We find both arguments unpersuasive.

Upon reviewing the record before us, we conclude that Harmonic's suggestions for modifying Haskell with an output switch or, alternatively, with the teachings of Rossmere, each suffices as an articulated reason with a rational underpinning to justify the legal conclusion of obviousness. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 417 (2007). For instance, to support combining the teachings of Haskell and Rossmere, Harmonic explains that:

> A person of ordinary skill in the art would be motivated to combine the teachings of Haskell with Rossmere, as doing so would be making use of a known component for a known use, and because Rossmere benefits Haskell in enabling Haskell to choose one input for use. Moreover, combining the teachings of Haskell and Rossmere, beyond reasons set forth above, would allow one to make use of the video output of Haskell in a

> manner "such that the user will not perceive any discontinuities in either the audio or the video channel outputs" as specifically recited in Rossmere. *See* Ex. 1009 at 2:45-46; Ex. 1002, ¶¶ 269-270.

Pet. 47. In our view, these statements suffice as an articulated reason with a rationale underpinning to support combining the teachings of Haskell and Rossmere.

Avid's argument that modifying Haskell's system with an output switch would change Haskell's principle of operation, or render Haskell inoperable for its intended purpose, is predicated on the notion that Haskell's principle of operation is to provide one or more separate outputs that correspond to its one or more separate inputs. However, Avid does not provide sufficient or credible evidence to support this general assertion. Moreover, Avid does not submit evidence or argument regarding the technological difficulties that may prevent one with ordinary skill in the art from making the proposed combinations. Absent contrary evidence, we are not convinced that modifying Haskell system in the manners proposed by Harmonic would change Haskell's principle of operation, or render Haskell inoperable for its intended purpose.

Finally, Avid contends that the combination of Haskell and Rossmere fails to teach a "controller coupled to the input switch, the decompression modules, and the output switch for selecting which decompression module will receive video data at the first predefined rate," as recited in independent claim 1, and similarly recited in independent claim 9. Prelim. Resp. 36. In particular, Avid argues that, even if an output switch were added to

Haskell's system, it would not be controlled by Haskell's switch controller 220 or system clock 212. *Id*. at 37. We find Avid's argument unpersuasive.

Harmonic takes the position that the switch controller 202 and system clock 212 are coupled to demultiplexer switch 203, indirectly coupled to decoders 208-1 through 208-N, and necessarily coupled to an output switch. Pet. 45 (citing to Ex. 1008, Figs. 2 and 3; Ex. 1002 ¶ 266). The cited paragraph in the declaration of Dr. Zeger simply reiterates the position taken by Harmonic in the petition with respect to the claimed "controller." Given that the switch controller 202 and system clock 212 directly or indirectly are coupled to both the demultiplexer switch 203 and decoders 208-1 through 208-N, one with ordinary skill in the art would have recognized that the switch controller 202 and system clock 212 are capable of controlling these components. In addition, Harmonic's position with respect to the switch controller 202 and system clock 212 is based on the addition of an output switch—taught by the decoder unit illustrated in Figure 1 of Haskell or, alternatively, taught by Rossmere—to Haskell's system. Avid does not provide a credible reason that explains why Haskell's switch controller 202 and system clock 212 are incapable of being coupled to a newly added output switch. As a result, we are persuaded that Harmonic provides sufficient evidence to support a finding that the combination of Haskell and Rossmere teaches the controller configurations required by independent claims 1 and 9.

Based on the record before us, Harmonic has demonstrated a reasonable likelihood of prevailing on its assertion that independent claims 1

and 9 are unpatentable under 35 U.S.C. § 103(a) over the combination of Haskell and Rossmere. The explanations provided by Harmonic as to how the combination of Haskell and Rossmere teaches the claimed subject matter recited in dependent claims 2-8 and 10-16 have merit and are otherwise unrebutted. As a result, Harmonic has demonstrated a reasonable likelihood of prevailing on its assertion that dependent claims 2-8 and 10-16 are unpatentable under 35 U.S.C. § 103(a) over the combination of Haskell and Rossmere.

B. 35 U.S.C. § 102(b) Ground of Unpatentability—Haskell

Claims 17-20

Harmonic contends that claims 17-20 are anticipated under 35 U.S.C. § 102(b) by Haskell. Pet. 52-58. In particular, Harmonic explains how Haskell allegedly describes the claimed features recited in these claims, and relies upon the Declaration of Dr. Zeger to support its positions. *Id*. We have considered Harmonic's explanations and supporting evidence, as well as Avid's arguments, but are not persuaded that Haskell accounts properly for "decompressing the selected first video data stream at a first rate for the duration of the first video data stream," as recited in independent claim 17.

Harmonic takes the position that Haskell describes "decompressing the selected first video data stream at a first rate for the duration of the first video data stream," as recited in independent claim 17. Pet. 53. In particular, Harmonic indicates that Haskell discloses that decoders 208-1 through 208-N decompress the video streams. *Id*. Based on that disclosure, Harmonic concludes that one with ordinary skill in the art would have

understood that decompression can occur for the duration of the stream. *Id*. (citing to Ex. 1008, Fig. 3, 13:46-48). Harmonic also indicates that Haskell discloses managing the rate for each decoder buffer separately. *Id*. (citing to Ex. 1008, 2:28-32, 2:41-44; Ex. 1002 ¶ 293).

In response, Avid contends that because Harmonic fails to demonstrate that Haskell expressly describes the disputed "decompressing" method step, Harmonic must rely upon the doctrine of inherency to establish anticipation under 35 U.S.C. § 102(b). Prelim. Resp. 40. Avid argues that Harmonic's conclusion that one with ordinary skill in the art would have recognized that decompression can occur for the duration of the stream is insufficient to establish that the disputed "decompressing" method step inherently is disclosed by Haskell. *Id*. at 41. Avid asserts that in order to establish inherency, decompression for the duration of the video stream must be the necessary result of Haskell's disclosure of decompressing video at different rates and separately managing the rate of each decoder buffer. *Id*. We agree with Avid that Harmonic improperly relied upon the doctrine of inherency when alleging that Haskell describes the disputed "decompressing" method step recited in independent claim 17.

"Inherency . . . may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (citations omitted). While Haskell relies upon disparate disclosures that may indicate that decompression occurs at a first rate for the duration of a first stream, mere probabilities or possibilities fall short of

demonstrating that Haskell necessarily describes decompressing a video stream at a first rate for the duration of that video stream, as is required for an anticipation rejection. Therefore, Harmonic improperly relied upon the doctrine of inherency when taking the position that Haskell describes "decompressing the selected first video data stream at a first rate for the duration of the first video data stream," as recited in independent claim 17.

Harmonic has not demonstrated a reasonable likelihood of prevailing on its assertion that independent claim 17 is anticipated under 35 U.S.C. § 102(b) by Haskell because Harmonic's position with respect to Haskell does not account properly for "decompressing the selected first video data stream at a first rate for the duration of the first video data stream," as recited in independent claim 17. Claims 18-20 directly depend from independent claim 17. For the same reasons discussed above with respect to independent claim 17, Harmonic has not demonstrated a reasonable likelihood of prevailing on its assertion that dependent claims 17-20 are anticipated under 35 U.S.C. § 102(b) by Haskell.

In footnote 6 on page 52 of the petition, Harmonic generally alleges an alternative ground of unpatentability for claims 17-20 that is based on the combination of Haskell and Rossmere. However, Harmonic's alternative ground of unpatentability fails to "specify where each element of the claim is found . . . ." 37 C.F.R. § 42.104(b)(4). For instance, Harmonic does not explain how Rossmere might remedy the deficiencies in Haskell, nor applies the combination of Haskell and Rossmere against the claim features recited in claims 17-20. "The Board may exclude or give no weight to the evidence

where a party has failed to state its relevance or to identify specific portions of the evidence that support the challenge." 37 C.F.R. § 42.104(b)(5). Therefore, we will not consider the combination of Haskell and Rossmere further because Harmonic does not apply these references to the claim features recited in claims 17-20.

C. 35 U.S.C. § 102(b) Ground of Unpatentability—Paik

Claims 17-20

Harmonic contends that claims 17-20 are anticipated under 35 U.S.C. § 102(b) by Paik. Pet. 38-40. Similar to its position with respect to Haskell, Harmonic concludes that one with ordinarily skill in the art would have understood that the decompression performed by Paik's decoders can occur for the duration of the stream and, therefore, Paik describes "decompressing the selected first video data stream at a first rate for the duration of the first video data stream," as recited in independent claim 17. *Compare* Pet. 39 *with* Pet. 53. As discussed above, we determined that Harmonic improperly relied upon the doctrine of inherency when taking the position that Haskell describes the disputed "decompressing" method step as recited in independent claim 17. That same analysis applies with respect to Paik. Therefore, Harmonic has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 17-20 are anticipated under 35 U.S.C. § 102(b) by Paik for essentially the same reasons discussed above with respect to Haskell.

In footnote 5 on page 38 of the petition, Harmonic generally alleges an alternative ground of unpatentability for claims 17-20 that is based on the combination of: (1) Paik and Haskell; (2) Paik and Rossmere; and (3) Paik, Haskell, and Rossmere. We will not consider the aforementioned combinations further because Harmonic does not apply these references to the claim features recited in claims 17-20. *See supra*.

D. 35 U.S.C. § 103(a) Grounds of Unpatentability—(1) APA; and (2) APA and Hang

Claims 17-20

Harmonic contends that claims 17-20 are unpatentable under 35 U.S.C. § 103(a) over: (1) APA; and (2) APA and Hang. Pet. 20, 26-27. Even though Harmonic acknowledges that independent claim 17 is directed to a method, it nonetheless contends that the claim limitations recited in independent claim 17 would be obvious in light of the rationale set forth with respect to the systems recited in independent claims 1 and 9. *Id*. Harmonic also asserts that the claim limitations recited in independent claim 17 are provided for during operation of the systems recited in independent claims 1 and 9. *Id*. (citing to Ex. 1002 ¶¶ 140-141, 201-202).

Independent claim 17, however, recites the following claim limitations:

> decompressing the remaining video data streams at a second rate prior to the end of the first video data stream; [and]

> repeating the selecting, decompressing, decompressing, and providing steps until all the video data streams have been provided to the output.

None of the claim limitations listed above are recited in the systems of independent claims 1 and 9. For example, independent claims 1 and 9 do not mention "decompressing the remaining video data streams at a second rate," nor do they mention repeating each method step "until all the video data streams have been provided to the output." Harmonic's petition fails to provide a sufficient and credible explanation as to how APA teaches the features recited in these claims limitations. As a consequence, Harmonic has not demonstrated a reasonable likelihood of prevailing on its assertion that claims 17-20 are unpatentable under 35 U.S.C. § 103(a) over: (1) APA; and (2) APA and Hang.

E. Remaining 35 U.S.C. § 103(a) Grounds of Unpatentability

Claims 1-16

Harmonic contends that claims 1-16 are unpatentable under 35 U.S.C. § 103(a) over: (1) APA; (2) APA and Hang; (3) Paik and Rossmere; and (4) Paik, Rossmere, and Haskell. Pet. 16-38. Those grounds of unpatentability are redundant to the grounds of unpatentability on which we initiate an *inter parties* review. Accordingly, we do not authorize an *inter partes* review on the remaining grounds of unpatentability asserted by Harmonic against claims 1-16 of the '291 patent. *See* 37 C.F.R. § 42.108(a).

IV. CONCLUSIONS

For the foregoing reason, we conclude that the information presented in the petition establishes that there is a reasonable likelihood that Harmonic would prevail in showing that claims 1-16 are unpatentable. However, we conclude that the information presented in the petition does not establish that there is a reasonable likelihood that Harmonic would prevail in showing that claims 17-20 are unpatentable.

The Board has not made a final determination under 35 U.S.C. § 318 with respect to the patentability of claims 1-16.

V. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted only as to claims 1-16 of the '291 patent as unpatentable under U.S.C. § 103(a) over the combination of Haskell and Rossmere;

FURTHER ORDERED that no other grounds of unpatentability are authorized for the *inter partes* review as to claims 1-16 of the '291 patent;

FURTHER ORDERED that an *inter partes* review is not instituted as to claims 17-20 of the '291 patent;

FURTHERED ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial. The trial will commence on the entry date of this decision; and

FURTHER ORDERED that an initial conference call with the Board is scheduled for 2PM on October 17, 2013. The parties are directed to the Office Trial Practice Guide, 77 *Fed. Reg*. 48756, 48765-66 (Aug. 14, 2012) for guidance in preparing for the initial conference call, and should come prepared to discuss any proposed changes to the Scheduling Order entered herewith and any motions the parties anticipate filing during the trial.

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