IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC,	)	
Plaintiffs/Counterclaim Defendants,	)	
v.	)	Civ. No. 13-453-SLR
TOSHIBA CORPORATION, TOSHIBA AMERICA, INC., TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC., and TOSHIBA AMERICA INFORMATION SYSTEMS, INC.,	)	
Defendants/Counterclaim Plaintiffs.	)	

MEMORANDUM ORDER

At Wilmington this 11th day of January, 2017, having reviewed the parties' supplemental papers (D.I. 565, 566, 568, 569) that were submitted consistent with the issues raised at the December 19, 2016 pretrial conference;

IT IS ORDERED, for the reasons discussed below, that Toshiba is not estopped from presenting the Fuse combination at trial, and Toshiba's request for reconsideration of claim construction of the '270 patent is denied.

Statutory Estoppel

1. Having reviewed the letters (D.I. 566, 568) and the case law submitted by the parties,[1] I conclude that my first look at the estoppel issue was incomplete. As I now understand the lay of the land, everyone agrees that estoppel applies to grounds for invalidity upon which the Board instituted review in the IPR proceeding, whether or not the Board addresses those grounds in its final decision ("instituted grounds"). I believe that there likewise can be no dispute that estoppel does **not** apply to invalidity grounds that were raised by a petitioner in an IPR, but rejected by the Board as instituted grounds (i.e., "noninstituted grounds"). *See Shaw*, 817 F.3d at 1300 (a denied ground never becomes part of the IPR and, therefore, could not have been raised during the IPR); *HP*, 817 F.3d at 1347 ("noninstituted grounds do not become a part of the IPR" and "could not be raised in the IPR; therefore "the estoppel provisions of § 315(e)(1) do not apply."). Which leaves us with the situation at bar, where the invalidity ground at issue (the Fuse combination) was never raised in the IPR, but reasonably could have been raised during the IPR ("litigation ground"). To the best of my knowledge, the Federal Circuit has not addressed this specific fact pattern. The PTAB has. In *Apotex*, the PTAB addressed two grounds, one that had been raised but not made part of the instituted trial, and one that was known but not raised in the IPR. Estoppel applied to the latter, but not the former. 2015 WL 5523393, at *4-5.[2]

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[1] *Shaw Indus. Grp., Inc. v. Automated Creel Sys., Inc.*, 817 F.3d 1293 (Fed. Cir. 2016); *H.P. Inc. v. MPHJ Tech. Inv., LLC*, 817 F.3d 1339 (Fed. Cir. 2016); *SAS Inst., Inc. v. ComplementSoft, LLC*, 825 F.3d 1351 (Fed. Cir. 2016); *Precision Fabrics Group, Inc. v. Tietex Int'l, Ltd.*, 2016 WL 6839394 (M.D. N.C. Nov. 21, 2016); *Apotex Inc. v. Wyeth LLC*, No. IPR2015-00873, 2015 WL 5523393 (P.T.A.B., Sept. 16, 2015).

[2] The reasoning in *Precision Fabrics* is not helpful, as the court held estoppel to apply to grounds that the "PTAB did not address . . . in its final decision," leaving the question of whether these grounds were noninstituted grounds (under *Shaw's* reasoning, estoppel would not apply) or simply never raised at all. 2016 WL 6839394, at *9.

2. In the absence of specific authority, it seems to me that I am left with two options, based on different policy considerations and with very different consequences. IV's reasoning leads to the conclusion that the PTAB is meant to be the invalidity arbiter of first resort and, therefore, a company that seeks an IPR must bring to the PTAB's attention every ground the company has reason to think might be relevant; otherwise, it will be estopped from pursuing that ground in litigation. That outcome appears to be inconsistent with all of the limitations imposed by the PTAB on IPR proceedings (e.g., page limits for petitions, 14 point type, and portrait-view claim charts)[3] and leaves for trial only those references initially rejected by the PTAB. On the flip side of the coin is Toshiba's reasoning, which leads to the conclusion that a company can play games between the PTAB (IPR) and the courts (litigation), asserting some references in connection with the IPR but reserving some for litigation. As I stated in my prior opinion on this matter, that outcome does not strike me as necessarily consistent with the notion of having a parallel administrative proceeding that is supposed to supplant litigation and provide a faster, cheaper, better resolution to patent disputes.

3. On the whole, since it is not my place to make policy decisions, I am not inclined to change my original decision, with the hopes that an appeal may clarify the issue for future judges in future cases. Therefore, Toshiba is not estopped from presenting the Fuse combination at trial.

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[3] Of course, the statute already places numerous constraints on IPR proceedings. IPR petitions may be filed within a limited timeframe. 35 U.S.C. §§ 311(c), 315(b). Also, the grounds raised in IPR petitions are limited to anticipation and obviousness. 35 U.S.C. § 311(b)

Reconsideration of '270 Patent Claim Construction

4. Toshiba requests reconsideration[4] of the claim construction of the term "redundancy bus"[5] that I addressed at summary judgment. (D.I. 565) During claim construction, Toshiba proposed that a "redundancy bus" is an "address bus that allows for the addressing of the redundant memory cells independent of the addressing of the primary memory cells through the primary address bus." (D.I. 183 at 2) I adopted Toshiba's construction. (D.I. 277 at 4) At summary judgment, Toshiba argued that "the [c]ourt's claim construction requires two address buses, a 'primary address bus' and a separate 'redundancy bus' that is independent from the primary address bus." (D.I. 434 at 7) IV disagreed, and I observed that "the parties dispute whether the primary and redundancy buses must be separate wires or if a multiplexed bus, i.e., a single wire, may satisfy the claims." (D.I. 559 at 28) Based upon the arguments presented and the claims in light of the specification, I clarified that "[i]n the '270 patent, both the address system and the primary and redundancy buses may be multiplexed." (D.I. 559 at 29)

5. Toshiba now argues that I made a "factual mistake . . . regarding the '270 patent specification's discussion of multiplexing." (D.I. 565 at 1) Specifically, Toshiba avers that: "[t]he court's ruling is premised upon a misreading of column 10:52-65 of the specification as teaching the use of a single multiplexed bus . . . . The specification never teaches combining the primary address bus and the redundancy bus into a single multiplexed bus." (D.I. 565 at 1-2) Here, Toshiba adds verbiage ("a single multiplexed bus") that is not found in either my prior opinion or the specification.

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[4] IV argues that this is a request for reconsideration of a claim construction argued in the motions for summary judgment and that Toshiba has presented no basis for reconsideration. (D.I. 569) I agree.

[5] Found in claims 1, 3, and 20 of the '270 patent.

6. In my memorandum opinion, I addressed the '270 patent 10:52-62, noting that the preferred embodiments disclose a non-multiplexed address bus and a non-multiplexed addressing scheme. (D.I. 559 at 28) In light of these disclosures in the specification, the relevant paragraph stands out:

> Alternatively, address bus 202 and redundancy address bus 301 may be multiplexed. In this case, row address bits alone would be pipelined through row address amplifier/buffers 401 and redundancy address amplifiers/buffers 402 from address bus 202 and redundancy address bus 301 respectively. Similarly, in a multiplexed address system, only column address bits would be pipelined through column address amplifiers/buffers 406 and redundancy column address amplifiers/buffers 408. In the case of redundancy addressing, redundancy address bits to redundant rows are pipelined along with the remaining row address bits through buffer/amplifiers 402 and redundancy address bits to redundant columns are pipelined along with the remaining column address bits through buffers/amplifiers 408.

('270 patent, 10:52-65) This paragraph discusses two different alternative embodiments: bus multiplexing and address multiplexing. The word "alternatively" prefaces a statement in the specification that the "address bus [] and redundancy address bus [] may be multiplexed." (*Id.*, 10:52-53) This is followed by a sentence beginning with "[s]imilarly, in a multiplexed address system." (*Id.*, 10:57) I cannot conclude, in light of the second sentence, that the first sentence does not disclose multiplexed primary and redundancy address buses. Therefore, Toshiba's request for reconsideration is denied.

United States District Judge